

## ABSTRACT OF THE DISCLOSURE

An electrical circuit generates both a differential data signal and a “squench,” or “out-of-band,” state over a differential signal pair by employing common-mode  
5 logic (CML) technology. In one embodiment of the invention, a CML buffer having true and complementary (inverted) data outputs drive the differential data signal onto the positive (‘p’) and negative (‘n’) signal lines of the differential pair. To implement the squench state, the true and complementary outputs of a two-input CML  
10 multiplexer are coupled with the corresponding outputs of the buffer. The data inputs of the multiplexer are driven by the data input signal driving the buffer, as well as the logical inversion of the data input signal. A squench state signal then drives an input selector of the multiplexer to impress the squench state over the differential signal pair when active.